Ordering number: EN1339D

Monolithic Linear IC

LA4145

0.6 to 0.9 W AF Power Amplifier for Radio Cassette Recorders

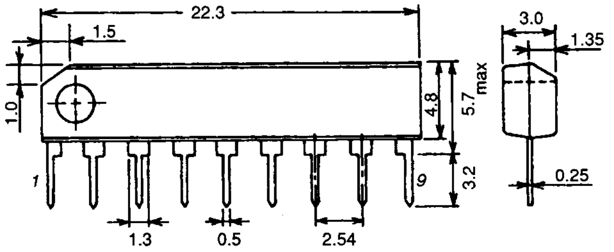
Features

- The LA4145 is especially suited for use in cassette tape recorder, radio-cassette, recorder, stereo cassette player applications.
- 0.6 W typ/V_{CC} = 6.0 V, R_L = 8 Ω, THD = 10%
  0.9 W typ/V_{CC} = 6.0 V, R_L = 4 Ω, THD = 10%
- Minimum number of external parts required
- Soft clip
- Small pop noise at V_{CC} ON/OFF mode
- Voltage gain fixed at 50 dB.
  An external resistor can be connected to reduce this value.

Package Dimensions

unit : mm

3017C-SIP9



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Quiescent mode	9	V
		Operating mode R_L = 8 Ω	8	V
Maximum output current	I_O peak		500	mA
Allowable power dissipation	Pd max	50 × 50 mm^2 with PCB	0.9	W
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		6	V
Recommended load resistance	R_L		4 to 8	Ω
Operating voltage range	V_{CC}		3.6 to 8	V

Operating Characteristics at Ta = 25°C, V_{CC} = 6.0 V, R_L = 8 Ω, Rg = 600 Ω, f = 1 kHz

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CCO}	LA4145		10	20	mA
Voltage gain	VG		48	50	52	dB
Output power	P_O	THD = 10%, R_L = 4 Ω		0.9		W
		THD = 10%, R_L = 8 Ω	0.45	0.6		W
Total harmonic distortion	THD	P_O = 0.1 W		0.2	1.0	%
Input resistance	r_i			30		kΩ
Output noise voltage	V_{NO}	Rg = 10 kΩ, B.P.F. = 20 Hz to 20 kHz		0.6	1.2	mV
Ripple rejection ratio	SVRR	Rg = 0, f_R = 100 Hz, V_R = 150 mV	–35	–40		dB

Proper care in changing voltage gain

An external resistor can be connected in series with the feedback capacitor at pin 2 to reduce the voltage gain. (See RNF-VG characteristic.)

IC usage notes

1. Maximum ratings
   If the IC is used in the vicinity of the maximum ratings, even a slight variation in conditions may cause the maximum ratings to be exceeded, thereby leading to breakdown. Allow an ample margin of variation for supply voltage, etc. and use the IC in the range where the maximum ratings are not exceeded.

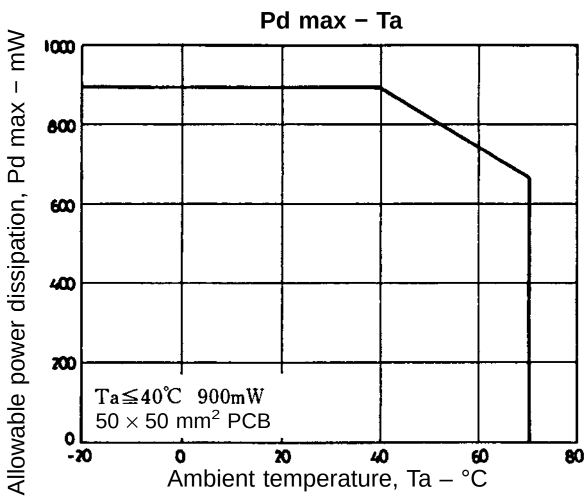
2. Pin-to-pin short
   If power is applied when the space between pins is shorted, breakdown or deterioration may occur. When mounting the IC on the board or applying power, make sure that the space between pins is not shorted with solder, etc.

3. Radio applications
   For use in radio applications, keep a good distance between IC and bar antenna.

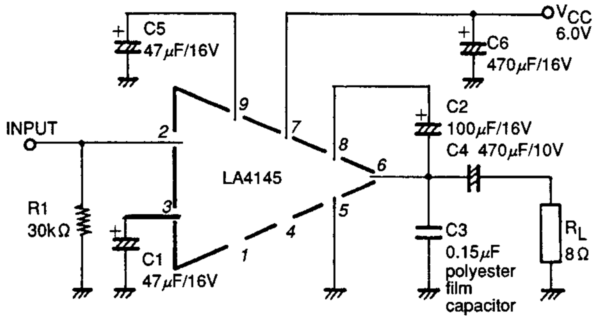
4. Printed circuit pattern
   When designing the printed circuit pattern, make the power supply, output, and ground lines thicker and shorter and determine the pattern and parts placement so that no feedback loop is formed between input and output. Place power capacitor C_6, oscillation blocking capacitor C_3 as close to the IC pin as possible to prevent oscillation from occurring. (See the sample printed circuit pattern.)

Description of external parts

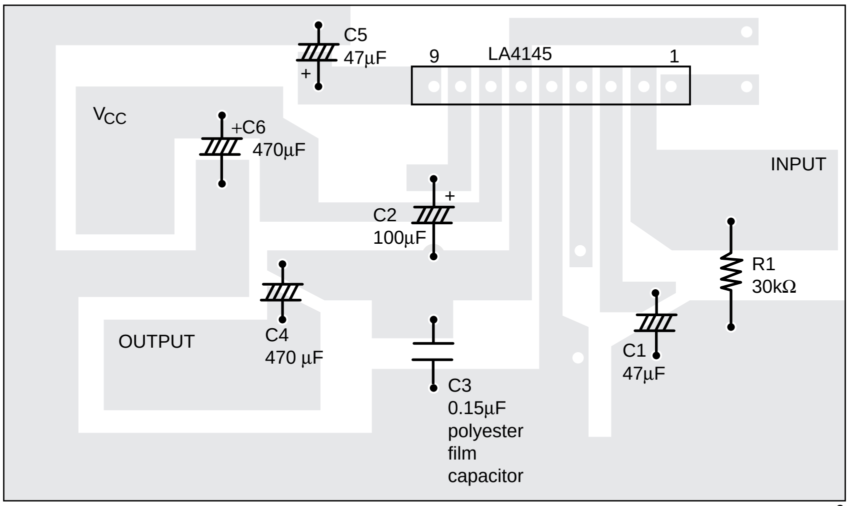
C_1 (47 µF)	Feedback capacitor (NF capacitor)	Low cutoff frequency f_L depends on this capacitor. f_L = 90 Hz for C_1 = 47 µF. Decreasing the capacitor value makes the starting time earlier.
C_2 (100 µF)	Bootstrap capacitor	
C_3 (0.15 µF)	Oscillation blocking capacitor	It is recommended to use a polyester film capacitor being good in temperature characteristic, high frequency characteristic.
C_4 (470 µF)	Output capacitor	
C_5 (47 µF)	Decoupling capacitor	Serves to reject ripple. The starting time depends on this capacitor. Increasing the capacitor value makes the starting time later.
C_6 (470 µF)	Power capacitor	Place as close to the power pin of the IC as possible.
R_1 (30 kΩ)	Input bias resistor	Serves to apply input bias. The input impedance almost entirely depends on this resistor value. If a variable resistor also serves for this purpose, this resistor can be omitted. In this case, it is recommended to use a resistor of 30 kΩ.



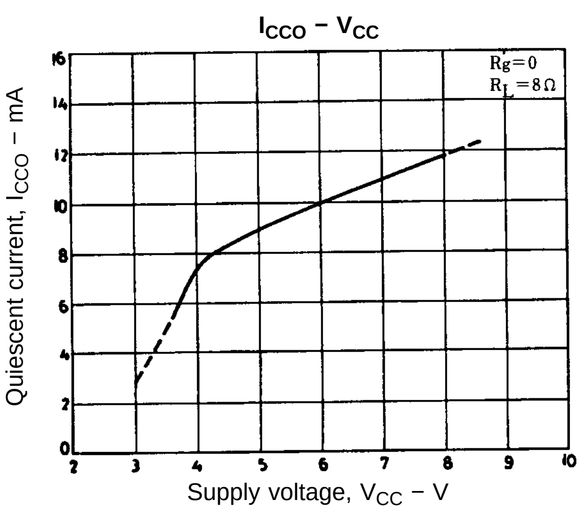
Sample Application Circuit: AF power amplifier

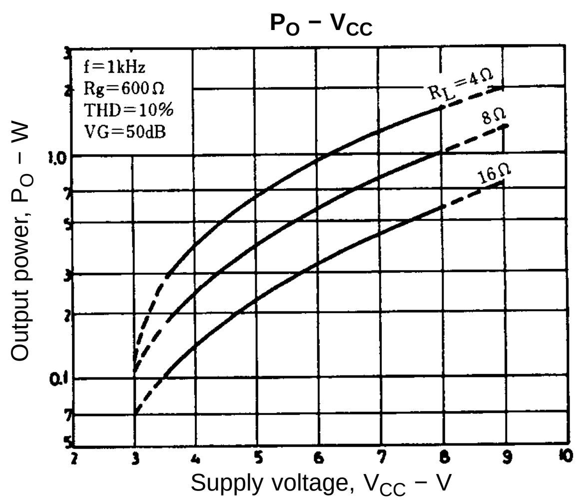


Sample Printed Circuit Pattern (Cu-foiled area)

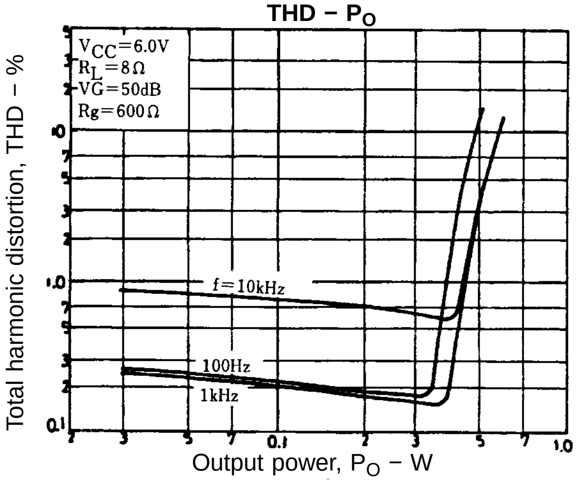


42.5 × 70.0mm²

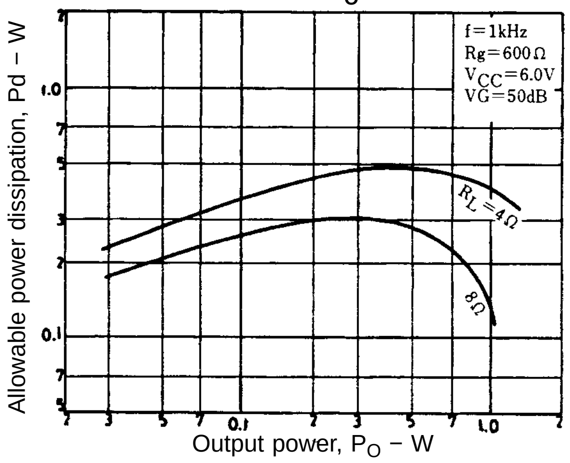




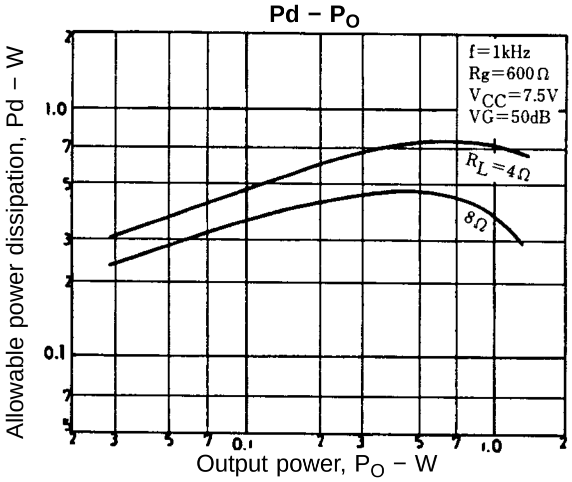
THD – P_O



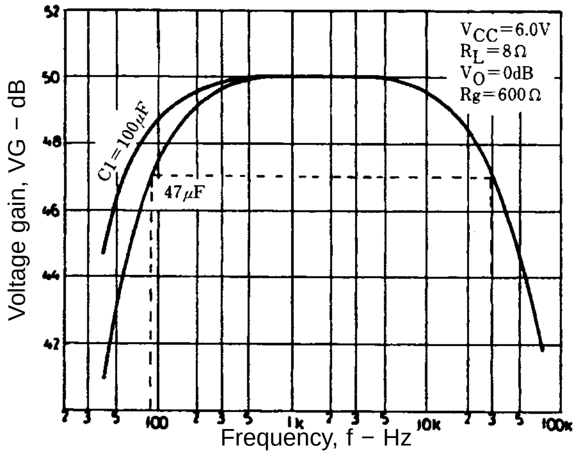
Pd – P_O



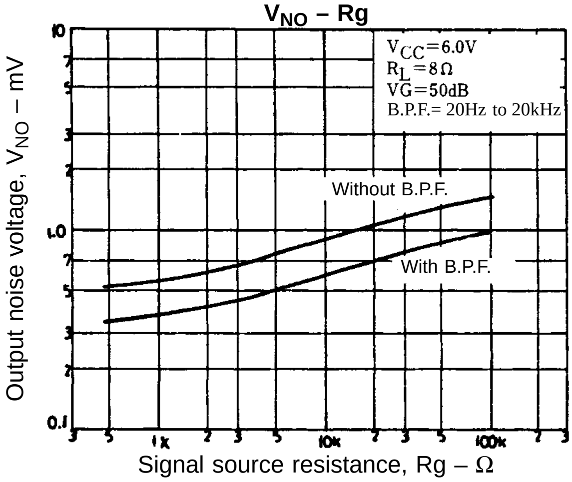
Pd – P_O



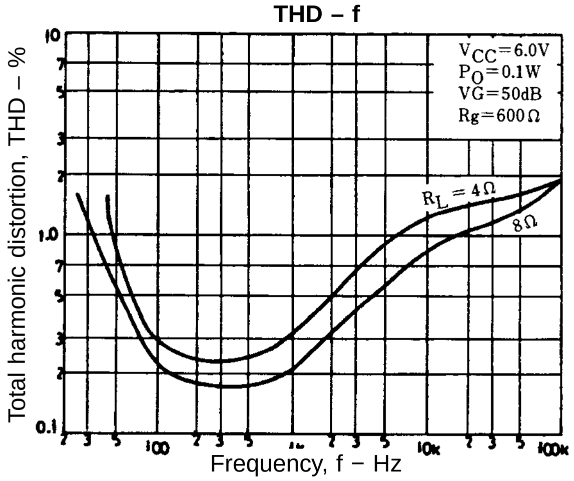
VG – f



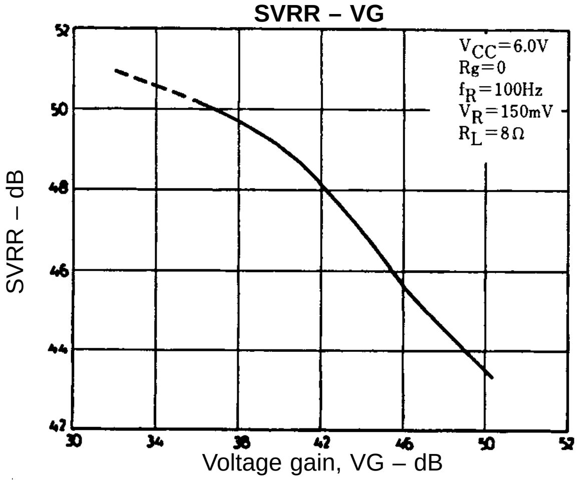
V_{NO} – Rg



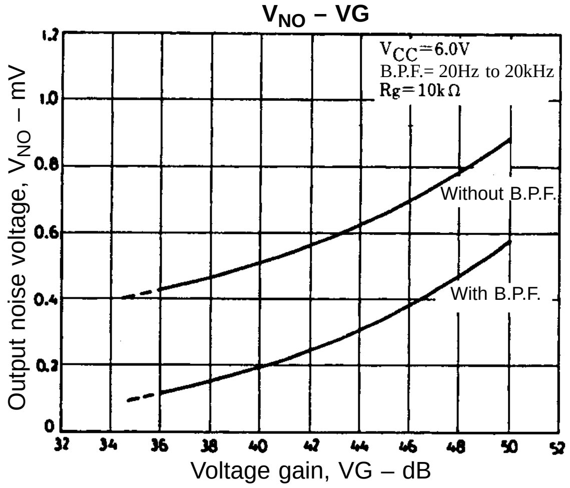
THD – f



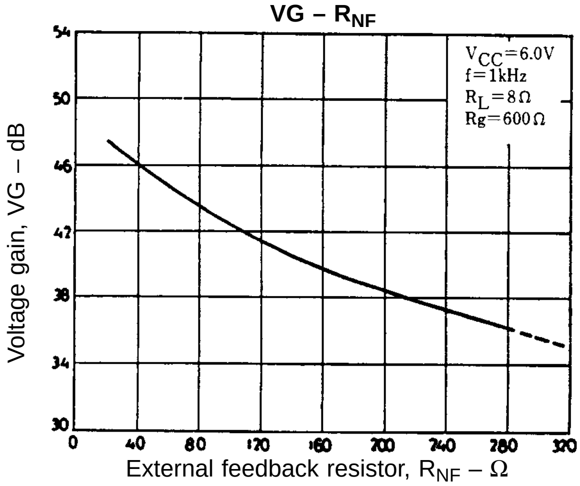
SVRR – VG



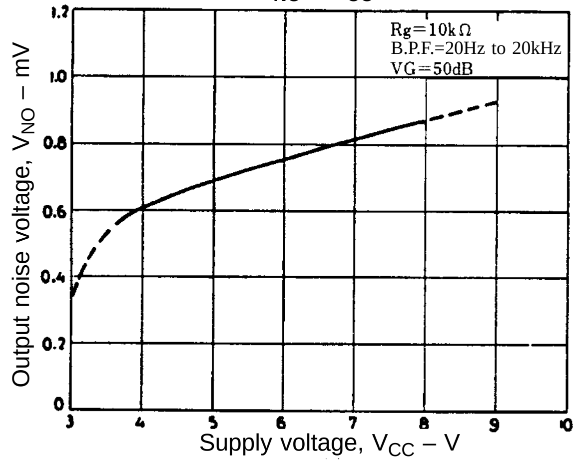
V_{NO} – VG



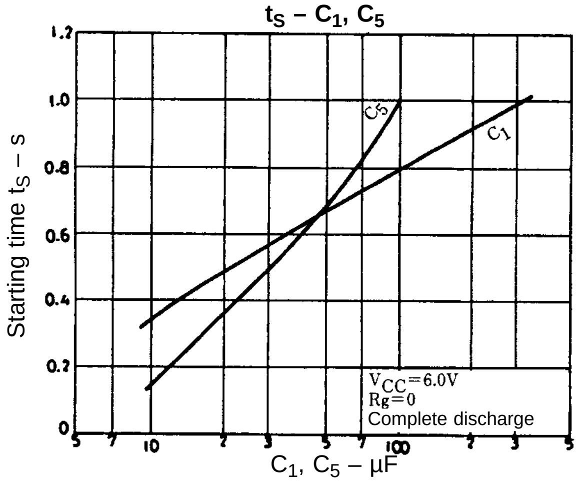
VG – R_{NF}



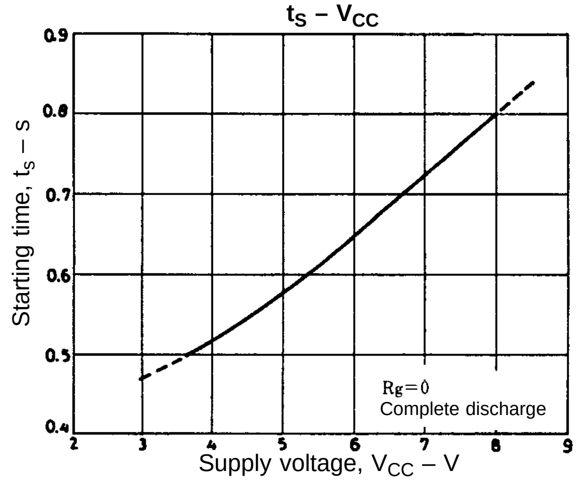
V_{NO} – V_{CC}



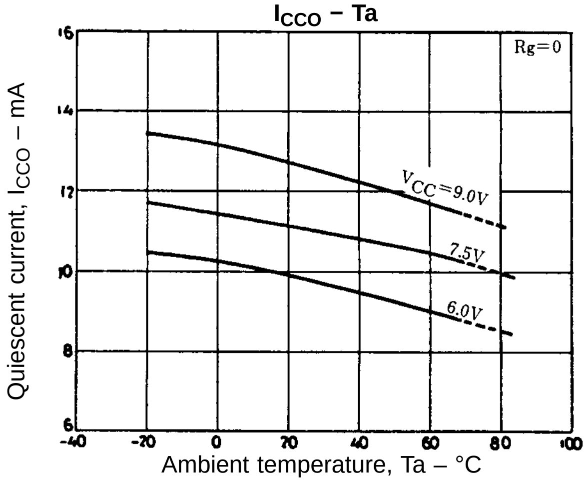
t_S – C_1, C_5



t_S – V_{CC}



I_{CCO} – Ta



P_O – Ta

